15. (Amended) The process of claim 13 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

A4
B1

16. (Amended) The process of claim 13 wherein the first polymeric dielectric material is inorganic and the second polymeric dielectric material is organic.

REMARKS

Applicants hereby respectfully re-traverse the election of species requirement made by the examiner under 35 U.S.C. 121. Applicants have previously provisionally elected the subject matter species of Embodiment 3 directed to Figures 2E, 5A-5F. This election was made with traverse. It should be noted that the Commissioner may statutorily require the election of inventions "If two or more independent and distinct inventions are claimed in one application." Applicants submit that the examiner has made no showing of distinctness between the subject matter species of Embodiments 1-4. It is therefore respectfully urged that the election of species requirement be rescinded.

Regarding the presently claimed invention, the examiner has objected to the specification, stating that the title is not descriptive of the invention. Applicants have amended the Title to now read "INTEGRATED CIRCUITS WITH BORDERLESS VIAS AND LOW DIELECTRIC-CONSTANT INTER-METAL DIELECTRICS". It is respectfully submitted that the title of the invention, as amended, is fully descriptive of the invention. Applicants therefore request that the examiner withdraw the objection.

The examiner has also objected to the term "a gaps" in claim 5, line 14. As the examiner suggested, Applicants have amended this term to now read "said gap". It is therefore respectfully requested that the objection to claim 5 be withdrawn.

The examiner has rejected claims 5-7 under 35 U.S.C. 112, second paragraph, as being indefinite. Applicants respectfully submit that this ground of rejection has been

overcome by the instant amendment. The examiner has stated that the term "additional layer of the first dielectric layer" is indefinite in claim 5, lines 9 and 13. Applicants have amended these portions of claim 5 to now read "an additional layer of the first polymeric dielectric *material*". The examiner also states that the phrase "a gap in at least one the recesses of the first dielectric layer at a side wall of a metal contact" is indefinite in claim 5, lines 11-12. Applicants have amended this portion of claim 5 to now read "a gap in at least one of the recesses of the *additional layer* of first polymeric dielectric *material* at a side wall of a metal contact". It is respectfully asserted that the 35 U.S.C. 112 rejection has been overcome by the instant amendment, and that the rejection should be withdrawn.

The examiner has rejected claims 5-6 under 35 U.S.C. 102 over Havemann. Applicants respectfully assert that this ground of rejection has been overcome.

The present invention relates to integrated circuits and the like. More particularly, the invention relates to the formation of borderless vias in intermetal dielectrics. The invention, as amended, claims an integrated circuit structure which comprises a substrate and a layer of a first polymeric dielectric material on the substrate, and a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material. A space is present between adjacent metal contacts, each space being filled with a second polymeric dielectric material. A recess is present in the filled spaces of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate. An additional layer of the first polymeric dielectric material is also present on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the additional layer of first polymeric dielectric material at a side wall of a metal contact. The integrated circuit structure also comprises at least one via extending through the additional layer of the first polymeric dielectric material extending to the top of at least one of the metal contacts and optionally to said gap. This via may be filled with at least one metal. It is an important feature of the invention that the first dielectric material and the second polymeric dielectric material

have substantially different etch resistance properties. In a preferred embodiment, the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

Havemann relates to the formation of semiconductor devices. In particular, in Figs. 2 and 4, Havemann describes a substrate which has an insulating layer 10 formed thereon. Patterned conductors 18 are formed on this insulating layer 10, and an organic-containing layer 22 is deposited thereon such that the tops of the conductors 18 remain exposed. An inorganic dielectric layer is formed thereon, and a via is formed through the inorganic dielectric and the organic-containing layer, to the level of the conductors 18. The inorganic dielectric layer is then etched down to the conductors 18 or the organic-containing layer 22, which act as an etch stop.

Indeed, Havemann teaches a semiconductor structure which is similar to that of the present invention. However, there are several key differences between Havemann and the present invention which render the invention patentably distinct from this cited reference. In particular, the present invention requires that the dielectric layers used according to the invention comprise a *polymeric* dielectric material. Preferred dielectric materials according to the invention include silicon containing polymers such as an alkoxysilane polymer, a silsesquioxane polymer, a siloxane polymer; a poly(arylene ether), a fluorinated poly(arylene ether), and the like.

In contrast, the insulating layer 10 of Havemann is composed of silicon dioxide. The inorganic dielectric layer 24 of Havemann is preferably composed of more than 95% silicon dioxide, silicon nitride, or combinations thereof. There is no teaching anywhere in Havemann that the insulating layer 10 or the inorganic dielectric layer 24 comprise a *polymeric* dielectric as taught by the present invention. Furthermore, Havemann actually *teaches away* from the present invention, by stating that polymeric dielectrics "have several drawbacks, including low temperature constraints which can limit further processing steps, lack of structural rigidity, poor heat transfer, and etching problems." (see col. 2, lines 18-21).

Havemann further fails to require that the insulating layer 10 and the inorganic layer 24 comprise the same material. The present invention teaches a first polymeric dielectric material layer and an "additional layer of the first polymeric dielectric material". Thus, according to the present invention, these two layers *must* be the same. Such is not taught by Havemann. It is submitted that the absence of these features of the presently claimed invention from the cited reference renders the invention patentably distinct from Havemann. Applicants respectfully urge that the 35 U.S.C. 102 rejection has been overcome and should be withdrawn.

The examiner has rejected claims 5-7 under 35 U.S.C. 102 over Grill et al. Applicants respectfully assert that this ground of rejection has been overcome. Grill et al. relates to interconnect structures having fluorine-containing dielectric materials. Indeed, Grill et al. teaches a structure having a substrate which is lined with a structure having various dielectric layers, insulating layers, conductive contacts, and vias, which is *similar* to those known in the art and taught by the present invention.

However, Applicants respectfully submit that Grill et al. fails to teach every aspect of the claimed invention. The present invention requires that the dielectric layers of the invention comprise a *polymeric* dielectric material. Examples of suitable and preferred polymeric dielectric materials are described above, and in the specification of the present invention. In contrast, Grill et al. *fails to teach* the use of polymeric dielectric materials *at all*. In fact, the word "polymer" does not appear anywhere in Grill et al.

The examiner asserts that the insulating fluorine-resistant capping layer 274, and additional layers 270,280 of Grill et al. are analogous to the first dielectric material layer and the additional layer of first dielectric material, respectively, of the present invention. However, it is submitted that the materials taught by Grill et al. for these layers are not polymeric. According to Grill, insulating capping materials include the insulating oxides, nitrides, or fluorides of the elements Ag, Al, Co, Cr, In, Ir, Mg, Mn, Sn, mixtures and

multilayers thereof, and amorphous silicon-containing carbon-based materials such as Si-containing DLC and Si-O-containing DLC.

The examiner also asserts that the fluorinated dielectric of Grill et al. is analogous to the second dielectric material layer of the present invention. Applicants submit that this is not the case, since none of Grill's fluorinated dielectric materials are polymeric. The fluorinated dielectric of Grill et al. is selected from the group containing fluorinated diamond like carbon (FDLC), fluorinated amorphous carbon (FLAC), FDLC or FLAC with additives selected from the group consisting of H, Si, Ge, O and N, fluorinated silicon glass (FSG), inorganic halogen-containing dielectrics and organic halogen-containing dielectrics.

It is submitted that the absence of a *polymeric dielectric material* of the present invention from the cited reference renders the present invention patentably distinct from Grill et al. It is therefore respectfully urged that the 35 U.S.C. 102 rejection has been overcome and should be withdrawn.

The undersigned respectfully requests re-examination of this application and believes it is now in condition for allowance. Such action is requested. If the examiner believes there is any matter which prevents allowance of the present application, it is requested that the undersigned be contacted to arrange for an interview which may expedite prosecution.

Respectfully submitted,

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I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office (FAX No. 703-308-7722) on September 23, 2002.

Richard S. Roberts

## APPENDIX

## MARKED-UP COPY OF SPECIFICATION PARAGRAPH

On page 1, in the Title :

[A FABRICATION METHOD OF] INTEGRATED CIRCUITS WITH BORDERLESS VIAS AND LOW DIELECTRIC-CONSTANT INTER-METAL DIELECTRICS

## MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) An integrated circuit structure which comprises

(a) a substrate;

(b) a layer of a first polymeric dielectric material on the substrate;

(c) a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material;

(d) a space between adjacent metal contacts, each space being filled with the first polymeric dielectric material;

(e) a recess in the filled spaces of the first polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate;

(f) a layer of a second polymeric dielectric material [layer] on at least some of the metal contacts and in the recesses on the filled spaces of the first polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the layer of the second polymeric dielectric material [layer] at a side wall of a metal contact;

(g) an additional layer of the first polymeric dielectric material on the layer of the second polymeric dielectric material [layer];

(h) at least one via extending through the additional layer of the first polymeric dielectric material [layer] and the layer of the second polymeric dielectric material [layer]

extending to the top of at least one of the metal contacts and optionally to [a gap] said gap;

wherein the first polymeric dielectric material and the second polymeric dielectric material have substantially different etch resistance properties.

3. (Amended) The structure of claim 1 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

4. (Amended) The structure of claim 1 wherein the first polymeric dielectric material is inorganic and the second polymeric dielectric material is organic.

5. (Amended) An integrated circuit structure which comprises

(a) a substrate;

(b) a layer of a first polymeric dielectric material on the substrate;

(c) a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material;

(d) a space between adjacent metal contacts, each space being filled with a second polymeric dielectric material;

(e) a recess in the filled spaces of the layer of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate;

(f) an additional layer of the first polymeric dielectric material [layer] on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the additional layer of first polymeric dielectric material [layer] at a side wall of a metal contact,

(g) at least one via extending through the additional layer of the first polymeric dielectric material [layer] extending to the top of at least one of the metal contacts and optionally to [a gaps] said gap;

wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties.

7. (Amended) The structure of claim 5 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

8. (Amended) The structure of claim 5 wherein the first polymeric dielectric material is inorganic and the second polymeric dielectric material is organic.

9. (Amended) A process for producing an integrated circuit structure which comprises
(a) providing a substrate;
(b) depositing a layer of a first polymeric dielectric material onto the substrate;
(c) forming a pattern of metal contacts on the layer of the first polymeric dielectric material including a space between adjacent metal contacts;
(d) depositing a layer of the first polymeric dielectric material on a top surface of the metal contacts and filling in the space between the metal contacts with the first polymeric dielectric material;
(e) removing the first polymeric dielectric material from the top surface of the metal contacts and removing an upper portion of the first polymeric dielectric material from the filled space between the metal contacts to form a recess;
(f) depositing a layer of a second polymeric dielectric material on the metal contacts and filling the recess with second polymeric dielectric material, wherein the first polymeric dielectric material and the second polymeric dielectric material have substantially different etch resistance properties;
(g) depositing an additional layer of the first polymeric dielectric material over the layer of the second polymeric dielectric material;
(h) depositing a layer of a photoresist on the additional layer of the first polymeric dielectric material;
(i) imagewise removing a portion of the photoresist over some of the metal contacts and optionally over a portion of at least one of the filled recesses adjacent to a side wall of a metal contact;

(j) removing the portion of the [layer of the] additional layer of the first polymeric dielectric material under the removed portion of the photoresist;

(k) removing the balance of the photoresist layer, and removing the portion of the second polymeric dielectric material under the removed portion of the additional layer of the first polymeric dielectric material until reaching at least one of the metal contacts and optionally reaching the space filled by the first polymeric dielectric material thus forming at least one via through the additional layer of the first polymeric dielectric material and through the layer of the second polymeric dielectric material.

10. (Amended) The process of claim 9 further comprising:

(n) depositing a layer of a barrier metal on the additional layer of the first polymeric dielectric material, and on inside walls and a floor of the at least one via;

(o) filling the at least one via with a fill metal and depositing a layer of a fill metal on the layer of the barrier metal;

(p) removing the fill metal layer, the barrier metal layer and optionally the additional layer of the first polymeric dielectric material.

11. (Amended) The process of claim 9 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

12. (Amended) The process of claim 9 wherein the first polymeric dielectric material is inorganic and the second polymeric dielectric material is organic.

13. (Amended) A process for producing an integrated circuit structure which comprises

(a) providing a substrate;

(b) depositing a layer of a first polymeric dielectric material onto the substrate;

(c) forming a pattern of metal contacts on the layer of the first polymeric dielectric material including a space between adjacent metal contacts;

(d) depositing a layer of a second polymeric dielectric material on a top surface of the metal contacts and filling in the space between the metal contacts with the second polymeric dielectric material;

(e) removing the second polymeric dielectric material from the top surface of the metal contacts and removing an upper portion of the second polymeric dielectric material from the filled space between the metal contacts to form a recess;

(f) depositing an additional layer of a first polymeric dielectric material on the metal contacts and filling the recess with first polymeric dielectric material, wherein the first polymeric dielectric material and the second polymeric dielectric material have substantially different etch resistance properties;

(g) depositing a layer of a sacrificial metal on the additional layer of the first polymeric dielectric material;

(h) depositing a layer of a photoresist on the layer of the sacrificial metal layer;

(k) imagewise removing a portion of the photoresist over some of the metal contacts and optionally over a portion of at least one of the filled recesses adjacent to a side wall of a metal contact;

(l) removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist;

(m) removing the balance of the photoresist layer, and removing the portion of the first polymeric dielectric material under the removed portion of the sacrificial metal layer until reaching at least one of the metal contacts and optionally reaching the space filled by the second polymeric dielectric material thus forming at least one via through the sacrificial metal layer and through the additional layer of the first polymeric dielectric material.

15. (Amended) The process of claim 13 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.

16. (Amended) The process of claim 13 wherein the first polymeric dielectric material is inorganic and the second polymeric dielectric material is organic.